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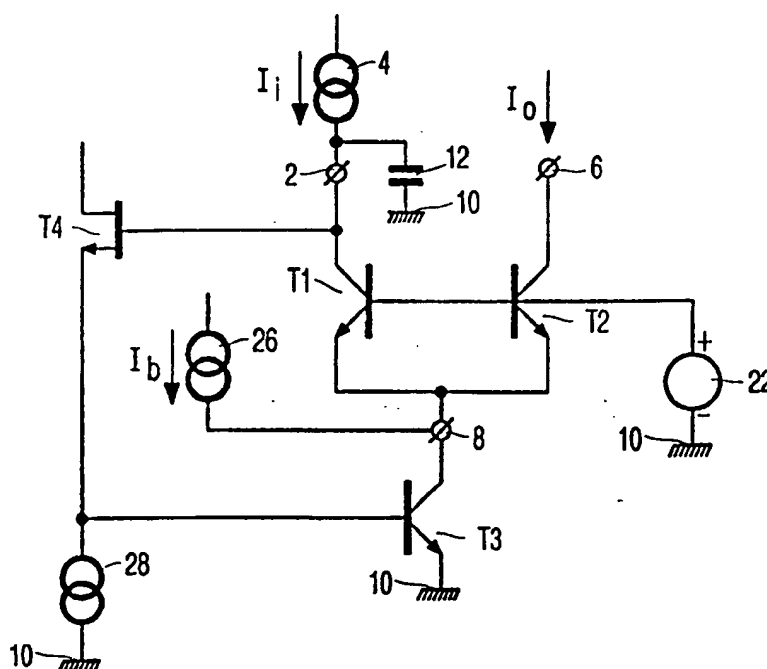
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(21) International Application Number: PCT/EP99/08639 (22) International Filing Date: 11 November 1999 (11.11.99) (30) Priority Data: 98203917.4 20 November 1998 (20.11.98) EP (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). (72) Inventors: GÜL, Hasan; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). FRAMBACH, Johannes, P., A.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). (74) Agent: HESSELMANN, Gerardus, J., M.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).		(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CURRENT MIRROR CIRCUIT

(57) Abstract

Current mirror circuit including a current input terminal (2), a current output terminal (6), a common terminal (8), a first transistor (T1) arranged between the current input terminal (2) and the common terminal (8), a second transistor (T2) arranged between the current output terminal (6) and the common terminal (8), a transconductance stage (TS) having an input terminal coupled to the current input terminal (2), and an output terminal coupled to the common terminal (8), and a bias source (22) for biasing the control electrodes of the first and second transistors (T1, T2). This configuration provides a large bandwidth independently of the input current, accurate current transfer and a single pole system.



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Current mirror circuit.

The invention relates to a current mirror comprising:

a first terminal for receiving an input current;

a second terminal for supplying an output current;

a common terminal ;

5 a first transistor having a control electrode, and having a main current path arranged between the first terminal and the common terminal ;

a second transistor having a control electrode connected to the control electrode of the first transistor , and having a main current path arranged between the second terminal and the common terminal .

10 Such a current mirror is known, for example, from United States Patent No. 4,462,005 and is shown in Fig. 1. In this well-known basic current mirror the interconnected control electrodes, in this case the bases, of the first transistor T1 and the second transistor T2 are connected to the first terminal which forms the current input terminal of the current mirror. The common terminal is connected to a reference terminal, in this case the negative supply
15 terminal which serves as signal ground. As will be explained hereinafter, the bandwidth of this known current mirror strongly depends on the input current due to the presence of an input capacitance C_i between the first terminal and the common terminal and of base-emitter capacitances C_{be} of the first and the second transistor T1 and T2. By adding degeneration resistors in series with the emitters of the first and the second transistor T1 and T2, as shown
20 in Fig. 2, the dependence on the input current can be avoided to some extent. However, this comes at the cost of a reduced bandwidth, an increased input impedance and a smaller voltage swing in comparison with to the basic current mirror of Fig. 1.

It is known to obtain an improvement in bandwidth by adding a gain stage GS as shown in Fig. 3. Fig. 4 shows gain stage formed by means of an emitter follower EF
25 between the first terminal and the interconnected control electrodes of the first and the second transistor T1 and T2. This improved current mirror still has a bandwidth which depends on the input current.

Therefore, it is an object of the invention to provide a current mirror with improved performance. To obtain the above object, according to the present invention, the current mirror of the type defined in the opening paragraph is characterized in that the current mirror further comprises:

- 5 a transconductance stage having an input terminal coupled to the first terminal , and having an output terminal coupled to the common terminal ;
and a bias source for biasing the control electrode of the first transistor and the control electrode of the second transistor .

The voltage at the first terminal is sensed by the transconductance stage which
10 drives the common terminal. In this way a feedback loop is created which makes the current through the first transistor equal to the input current, thus providing a low input impedance. The first and the second transistor, assuming that they are bipolar transistors are, in common base configuration and provide a large bandwidth. Advantageous embodiments are defined in the dependent Claims.

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These and other aspects of the invention will be described and explained with reference to the appended drawings, in which:

- Figure 1 is a circuit diagram of a known current mirror;
20 Figure 2 is a circuit diagram of a known current mirror;
Figure 3 is a circuit diagram of a known current mirror;
Figure 4 is a circuit diagram of a known current mirror;
Figure 5 is a circuit diagram of a first embodiment of a current mirror in accordance with the invention;
25 Figure 6 is a circuit diagram of a second embodiment of a current mirror in accordance with the invention;
Figure 7 is a circuit diagram of a third embodiment of a current mirror in accordance with the invention; and
Figure 8 is a circuit diagram of a fourth embodiment of a current mirror in
30 accordance with the invention.

In these Figures parts having the same function or purpose are denoted by the same references.

Figure 1 shows a circuit diagram of the well-known basic current mirror. Bipolar transistors are shown which each have an emitter and a collector which define the main current path of the transistor, and which each have a base which acts as a control electrode for controlling the current through the main current path. The current mirror has a first terminal 2 for receiving an input current I_i from an input current source 4, a second terminal 6 for supplying a mirrored output current I_o , and common terminal 8 which is connected to signal ground 10. The main current path of a first transistor T1 is arranged between the first terminal 2 and the common terminal 8, and the main current path of a second transistor T2 is arranged between the second terminal 6 and the common terminal 8. The emitters of the transistors T1 and T2 are connected to the common terminal 8. The bases of the transistor T1 and T2 are interconnected and the interconnected bases are connected to the first terminal 2. The current mirror has an input capacitor 12 between the first terminal 2 and ground 10.

The DC current transfer characteristic of the current mirror is:

$$I_o = I_i \left(1 - \frac{2}{\beta + 2} \right) \quad (1)$$

where β is the current gain of the transistors T1 and T2. The bandwidth f_h of this current mirror strongly depends on the input current I_i and can be calculated with the following equation (2):

$$f_h = \frac{g_m}{2\pi \cdot (C_i + 2C_{be})} = \frac{I_i}{2\pi \cdot (C_i + 2C_{be}) \cdot V_T} \quad (2)$$

where $g_m = I_i/V_T$ is the small signal transconductance of the transistor T1, C_i the capacitance of input capacitor 12, C_{be} the base-emitter capacitance of the transistors T1 and T2 and V_T the thermal voltage of a bipolar transistor. From equation 2 it is apparent that the bandwidth f_h is directly proportional to the input current I_i . This dependence can be reduced by applying emitter degeneration as shown in Figure 2. Degeneration resistors 14 and 16 are arranged in the emitter leads of the transistors T1 and T2, respectively. The bandwidth f_h for this configuration can be calculated with the following equation:

$$fh = \frac{1}{2\pi \cdot (C_i + 2C_{be}) \cdot (R_e + r_e)} = \frac{1}{2\pi \cdot (C_i + 2C_{be}) \cdot \left(R_e + \frac{V_T}{I_i}\right)} \quad (3)$$

where $r_e = 1/g_m$ of the transistor T1, and R_e the resistance of the degeneration resistor 14. If $R_e \gg r_e$, the bandwidth fh is mainly determined by the values of the capacitors and the degeneration resistor. The reduced input current dependence comes at the cost of a smaller bandwidth, an increased input impedance and a smaller voltage swing in comparison with the basic current mirror of Figure 1.

Figure 3 shows a known improved current mirror. The direct connection between the first terminal 2 and the interconnected bases is replaced with a gain stage GS, which has a non-inverting input connected to the first terminal 2, an inverting input connected to a reference voltage source 18 and an output connected to the interconnected bases. The input impedance r_i of this current mirror is given by:

$$r_i = \frac{1}{A \cdot g_{m1}} = \frac{1}{A} \cdot \frac{V_T}{I_i} \quad (4)$$

where A is the gain of the gain stage GS and g_{m1} the transconductance of the transistor T1. The input impedance r_i together with the capacitance C_i of the input capacitor 12 form a pole which determines the bandwidth fh of the current mirror, and is given by:

$$fh = \frac{1}{2\pi \cdot C_i \cdot r_i} = \frac{A \cdot I_i}{2\pi \cdot C_i \cdot V_T} \quad (5)$$

20

Compared with the bandwidth of the basic current mirror in equation 2, the bandwidth fh has increased owing to the gain A and the missing capacitance C_{be} , but is still proportional to the input current I_i . Again, emitter degeneration can be applied just as in the basic current mirror at the same cost of bandwidth, input impedance and voltage swing.

25

Figure 4 shows a version of the current mirror of Figure 3 in which the gain stage is an emitter follower transistor EF which has its base connected to the first terminal 2, its emitter connected to the interconnected bases of the transistors T1 and T2 and to a bias current source 20. Owing to the high gain A the DC transfer characteristic of the current mirror of Figure 3 is:

30

$$I_o = I_i \quad (5a)$$

while the DC current gain of the current mirror of Figure 4 is given by:

$$I_o = \left(I_i - \frac{I_e}{\beta + 1} \right) \cdot \left(1 - \frac{2}{\beta^2 + 1} \right) \quad (5b)$$

where I_e is the current of bias current source 20.

Figure 5 shows a current mirror in accordance with the invention. The interconnected bases of the transistors T1 and T2 are biased by a bias source 22. The current mirror further has a transconductance stage TS which has an inverting input coupled to the first terminal 2, a non-inverting input to a bias source 24 and a current output to the common terminal 8. The voltage at the first terminal 2 is sensed by the transconductance stage TS, which drives the emitter of transistor T1. The feedback loop thus formed adjusts the current through transistor T1 until it is equal to the input current I_i . The current through transistor T1 is copied to the second terminal 6 by the transistor T2. The DC current transfer characteristic of this arrangement therefore is the same as given in equation 5a. The transistors T1 and T2 are operated in common-base configuration and thus have a large bandwidth. Assuming that the transconductance stage TS also has a large bandwidth, which is generally the case, the dominant pole is located at the first input terminal 2 of the current mirror. As a result, this configuration offers the advantageous possibility of a single pole design.

The input resistance r_i of the Figure 5 current mirror is given by:

$$r_i = \frac{2}{g_m} \quad (6)$$

25

where g_m is the transconductance of the transconductance stage TS. The factor 2 in the equation 6 is due to the fact that the output current of the transconductance stage TS is halved by the transistors T1 and T2. The input resistance r_i and the input capacitance C_i form a pole which dictates the bandwidth f_h of the Figure 5 current mirror. This bandwidth is given by:

30

$$f_h = \frac{1}{2\pi \cdot C_i \cdot r_i} = \frac{g_m / 2}{2\pi \cdot C_i} \quad (7)$$

If the transconductance g_m is independent of the input current I_i , the bandwidth f_h is also independent of the input current.

Figure 6 shows an example of the transconductance stage TS with a transistor T3, which has its base coupled to the first terminal 2, its collector coupled to the common terminal 8 and its emitter coupled to ground 10. A bias current source 26 is also coupled to the common terminal 8 to provide a bias current I_b . The transconductance g_m of the transistor T3 is made independent of the input current I_i by adding the bias current I_b to the collector of transistor T3. In that case the transconductance g_m of the transistor T3 is given by:

10

$$g_m = \frac{I_b + 2I_i}{V_T} \quad (8)$$

By making the bias current I_b much larger than the input current I_i the input impedance will not change significantly with the input current I_i . It is to be noted that the extra bias current I_b does not flow through the actual current mirror T1-T2 and does not affect the output current I_o . In other words, the current mirror transfer characteristic and the input impedance can be optimized independently of each other. Because the input impedance, together with the input capacitor 12, determines the bandwidth, the bandwidth is also insensitive to the input current variations and can be optimized separately. The DC current transfer characteristic of the Figure 6 current mirror is given by:

20

$$I_o = \left(I_i - \frac{I_b}{\beta} \right) \cdot \left(1 - \frac{2}{\beta} - \frac{2}{\beta^2} \right) \quad (9)$$

Instead of directly coupling the base of the transistor T3 to the first terminal 2, an emitter follower transistor T4 can be placed between them as shown in Figure 7. The base of the transistor T4 is coupled to the first terminal 2 and the emitter of the transistor T4 drives the base of the transistor T3. A bias current source 28 supplies bias current to the emitter of transistor T4. This configuration with the emitter follower transistor T4 provides a larger voltage swing at the first terminal 2 within the mirror circuit itself at the cost of a higher DC input voltage level. Figure 8 shows an alternative configuration in which transistor T4 is a MOSFET, which has the advantage that no current is drawn from the first terminal 2, resulting

in a nearly perfect current mirror configuration with a 1 to 1 ratio between input current I_i and output current I_o (assuming equal transistors T1 and T2).

5 In the embodiments mainly bipolar transistors are shown. However, instead of bipolar transistors unipolar or MOSFET transistors can be used. In that case the gate, source and drain of the unipolar transistor substitute respectively the base, emitter and collector, of the bipolar transistor. Multiple outputs are possible by providing copies of the transistor T2 between the common terminal 8 and additional second terminals 6.

CLAIMS:

1. A current mirror comprising:
a first terminal (2) for receiving an input current;
a second terminal (6) for supplying an output current;
a common terminal (8);
5 a first transistor (T1) having a control electrode, and having a main current path arranged between the first terminal (2) and the common terminal (8);
a second transistor (T2) having a control electrode connected to the control electrode of the first transistor (T1), and having a main current path arranged between the second terminal (6) and the common terminal (8),
10 characterized in that the current mirror further comprises:
a transconductance stage (TS) having an input terminal coupled to the first terminal (2), and having an output terminal coupled to the common terminal (8);
and a bias source (22) for biasing the control electrode of the first transistor (T1) and the control electrode of the second transistor (T2).
15
2. A current mirror as claimed in claim 1, wherein the transconductance stage comprises a third transistor (T3) having a control electrode coupled to the first terminal (2), and having a main current path coupled between the common terminal (8) and a reference terminal (10).
20
3. A current mirror as claimed in claim 2, further comprising a buffer stage (T4) arranged between the first terminal (2) and the control terminal of the third transistor (T3).
4. A current mirror as claimed in claim 3, wherein the buffer stage comprises a
25 fourth transistor (T4) operating as a voltage follower, the fourth transistor having a control electrode coupled to the first terminal (2), and having main electrode coupled to the control electrode of the third transistor (T3).

5. A current mirror as claimed in claim 4, wherein the first to the third transistor (T1, T2, T3) are bipolar transistors and the fourth transistor (T4) is a MOSFET transistor.

6. A current mirror as claimed in claim 2, 3, 4, or 5, further comprising a bias
5 current source (26) coupled to the common terminal (8) to supply bias current to the common terminal (8).

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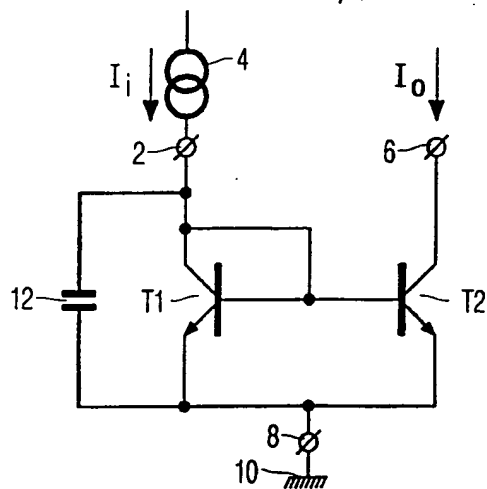


FIG. 1

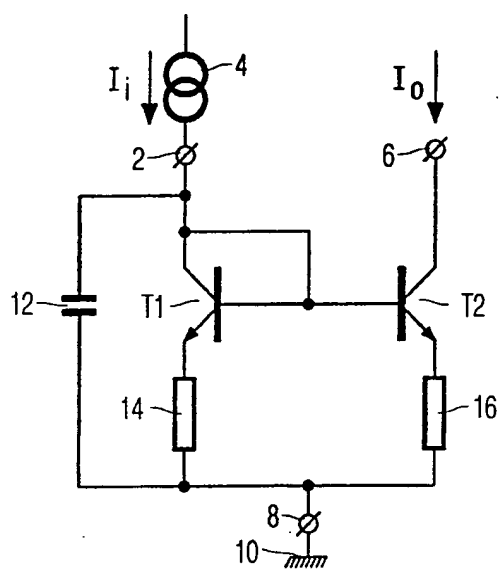


FIG. 2

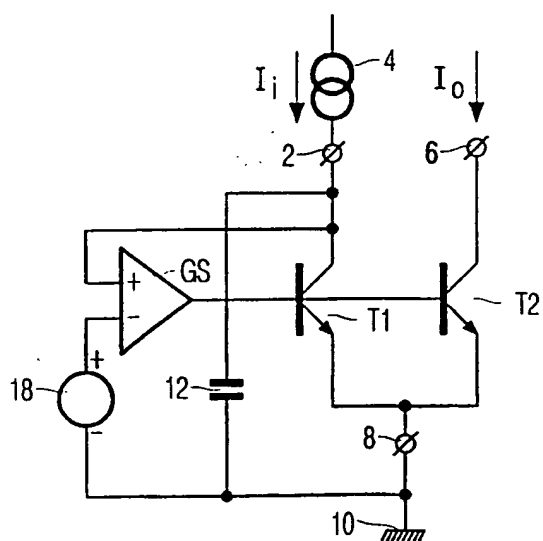


FIG. 3

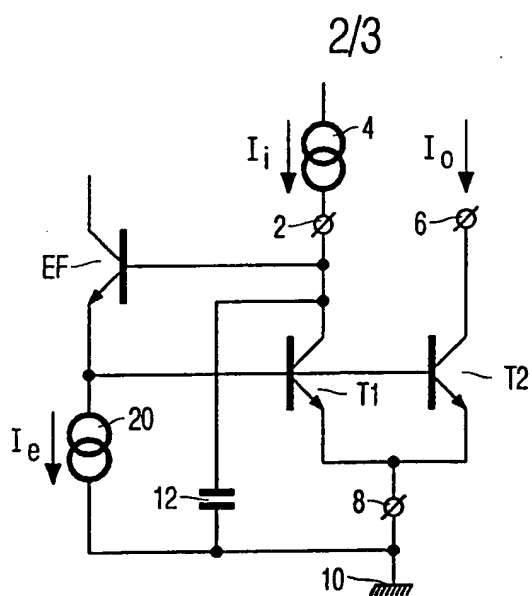


FIG. 4

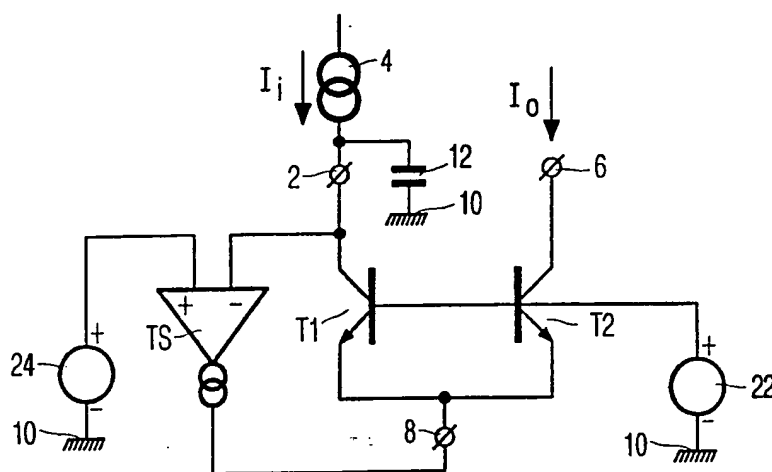


FIG. 5

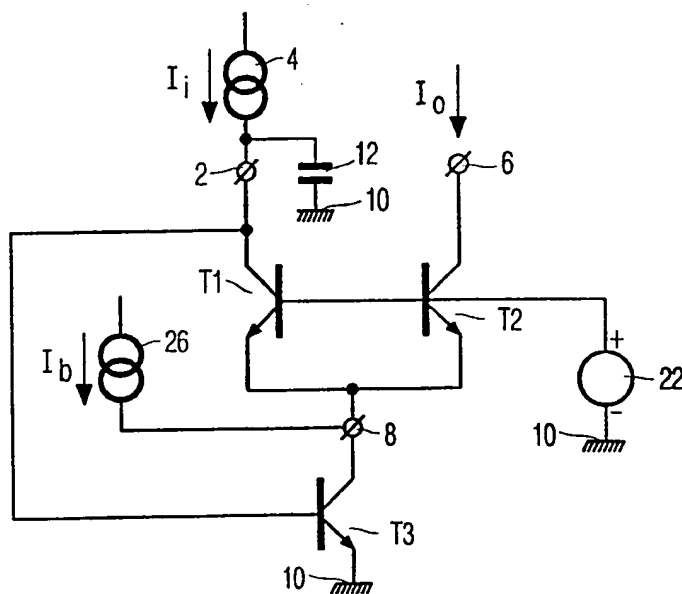


FIG. 6

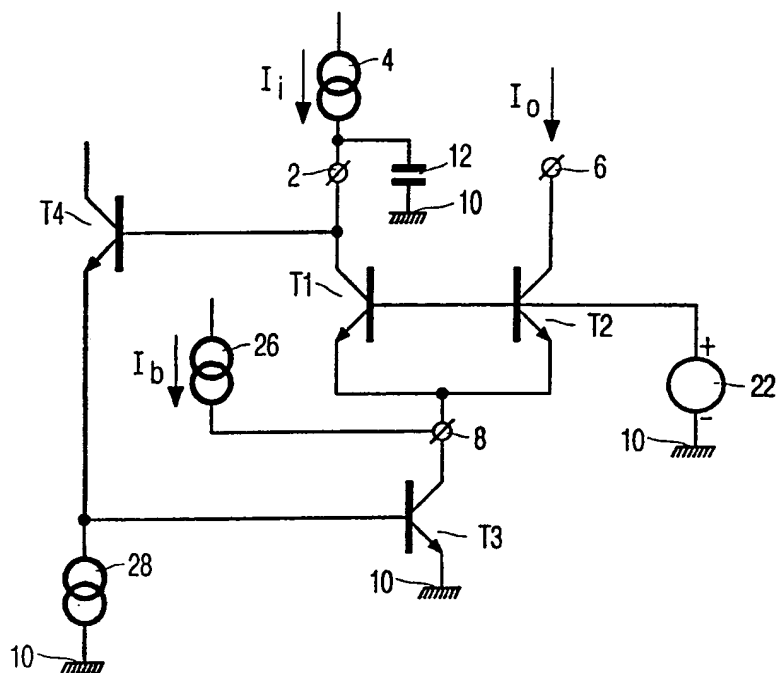


FIG. 7

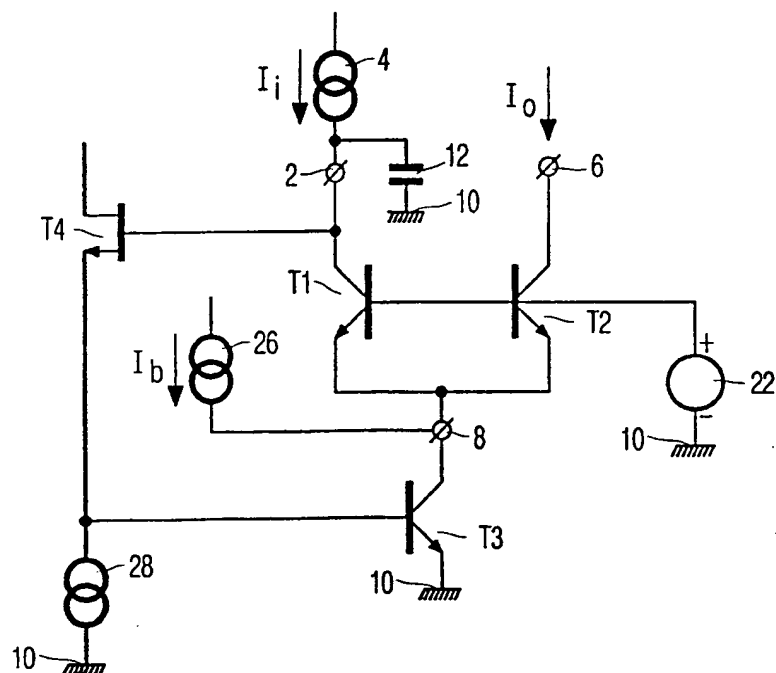


FIG. 8

INTERNATIONAL SEARCH REPORT

Inter. and Application No.

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G05F3/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G05F

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 323 795 A (HOLLOWAY PETER R ET AL) 6 April 1982 (1982-04-06) the whole document —	1-6
A	US 4 525 682 A (LAI STEPHEN H ET AL) 25 June 1985 (1985-06-25) the whole document —	1-6
A	US 4 769 619 A (TAYLOR STEWART S) 6 September 1988 (1988-09-06) abstract —	1-6
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A	<p>US 5 789 981 A (BROOKS TODD L ET AL) 4 August 1998 (1998-08-04) abstract</p> <p>_____</p>	1-6

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. nal Application No

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